What I claim as my invention is:

1. An application specific integrated circuit comprising;

an internal bus operating at a first clock frequency, and

a bridge coupling signals from said internal bus to an off-chip device operating at a second clock frequency.

2. The apparatus of Claim 1 wherein said bridge comprises:

a clock divider having an input receiving said first frequency and an output providing a clock signal at said second clock frequency,

a register storing and coupling data between said internal bus and said off-chip device, and

ready control logic modifying a HREADY signal to delay read and write cycles on said internal bus to accommodate data transfers on said off-chip device at said second clock frequency.

3. The apparatus of Claim 2 further comprising a configuration register storing a variable identifying said second frequency.

4. The apparatus of Claim 3 further comprising reset control logic maintaining an HRESETn signal to said off-chip device in an active state until said configuration register is loaded with said variable.

5. The apparatus of Claim 3 further comprising bus access control logic suppressing the HBUSREQ signal from said internal bus when said second frequency is different from said first frequency.

6. The apparatus of Claim 3 further comprising bus access control logic suppressing the HBUSGRANT signal from said off-chip device when said second frequency is different from said first frequency.

7. The apparatus of Claim 3 wherein said configuration register stores addresses assigned to said off-chip device.

8. The apparatus of Claim 1 wherein said off-chip device operates at first voltage levels representing logical ones and zeros which are different from second voltage levels representing logical ones and zeros at which the internal bus operates, further comprising input output buffers converting input and output signals between said first and second voltage levels.

9. A method for coupling signals from an internal bus on an integrated circuit to an off-chip device, comprising:

detecting the start of a bus write cycle on the internal bus,

comparing the address signal from the internal bus to addresses which are assigned to the off-chip device,

if an allowable address is detected, loading data from the internal bus into a register and deasserting an HREADY signal on the internal bus, and

driving the data stored in the register to the off-chip device.

10. The method of Claim 9 further comprising,

detecting assertion of an HREADY signal from the off-chip device and asserting the HREADY signal on the internal bus.

11. The method of Claim 9 wherein said integrated circuit includes a register for storing addresses assigned to said off-chip device.

12. The method of Claim 9 wherein the internal bus operates at a first clock frequency, said off-chip device operates at a second clock frequency, said integrated circuit includes a register for storing a variable identifying the difference between said first and second clock frequency, further comprising the step of dividing said first clock frequency to generate said second clock frequency and providing said second clock frequency to said off-chip device.

13. A method for coupling signals from an off-chip device to an internal bus on an integrated circuit, comprising:

detecting the start of a bus read cycle on the internal bus,

comparing the address signal from the internal bus to addresses which are assigned to the off-chip device,

if an allowable address is detected, loading data from the off-chip device into a register and deasserting an HREADY signal on the internal bus, and

driving the data stored in the register onto the internal bus.

14. The method of claim 13 further including;

asserting the HREADY signal on the internal bus.

15. The method of Claim 13 wherein said integrated circuit includes a register for storing addresses assigned to said off-chip bus.

16. The method of Claim 13 wherein the internal bus operates at a first clock frequency, said off-chip bus operates at a second clock frequency, said integrated circuit includes a register for storing a variable identifying the difference between said first and second clock frequency, further including the

step of dividing said first clock frequency to generate said second clock frequency and providing said second clock frequency to said off-chip bus.

17. An application specific integrated circuit comprising;

an internal bus operating at a first clock frequency ,

means for coupling signals from said internal bus to an off-chip device operating at a second clock frequency.

18. The apparatus of Claim 17 wherein said means for coupling includes;

an input for receiving a clock signal at said first clock frequency and an output for providing a clock signal at said second clock frequency.

19. The apparatus of Claim 18 wherein said means for coupling includes means for storing a variable identifying said second clock frequency.

20. The apparatus of Claim 17 wherein said means for coupling includes storage means for storing and coupling data between said internal bus and said off-chip device, and means for modifying a HREADY signal on said internal bus to accommodate data transfers with said off-chip device at said second clock frequency.